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STATE-DELAYED TECHNIQUE AND SYSTEM TO REMOVE TONES OF DYNAMIC ELEMENT MATCHING

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CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Patent Application No. 10/434,220, filed May 9, 2003, which is now a U.S. Patent 6,720,897 entitled State-Delayed Technique and System to Remove Tones of Dynamic Element Matching, incorporated herein by reference in its entirety.

This application is related to U.S. Patent Application No. 10/354,159, filed January 30, 2003, entitled HARDWARE-EFFICIENT IMPLEMENTATION OF DYNAMIC ELEMENT MATCHING IN SIGMA-DELTA DAC'S, incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

[0001] In high resolution digital-to-analog converters (DACs), performance metrics such as linearity and noise are nominally determined by the matching of parameters derived from physical quantities in the construction of the DACs on an integrated circuit (IC), such as width, length, thickness, doping, etc. As a general rule, for each additional bit of performance in the DAC, parameter matching needs to be twice as tight. This translates to an increase by a factor of four in the IC area required by the DAC. When the DAC resolution is in the 16-bit range, it is no longer practical or economical to use size alone to achieve the required matching.

[0002] Over-sampled (delta-sigma or Δ–Σ) DACs alleviate the need for raw matching using single-bit conversion (so called 1-bit DACs in CD players). A single-bit DAC has only two points in a transfer function of the DAC, and thus is inherently linear. The function of a Δ–Σ modulator with a one-bit quantizer is to approximate a high-resolution, low-frequency signal with a high-